Digital Switching

UNIT 2
Lecture 1

Advantages and Issues of Digital Switching

There are both economic and technical advantages to digital switching; in this context we refer to PCM switching. The economic advantages of time-division PCM switching include the following:

- There are notably fewer equivalent cross-points for a given number of lines and trunks than in a space-division switch.
- A PCM switch is of considerably smaller size.
- It has more common circuitry (i.e., common modules).
- It is easier to achieve full availability within economic constraints.

The technical advantages include the following:

- It is regenerative (i.e., the switch does not distort the signal; in fact, the output signal is “cleaner” than the input).
- It is noise-resistant.
- It is computer-based and thus incorporates all the advantages of SPC.
- The binary message format is compatible with digital computers. It is also compatible with signaling.
- A digital exchange is lossless. There is no insertion loss as a result of a switch inserted in the network.
- It exploits the continuing cost erosion of digital logic and memory; LSI, VLSI, and VHSIC insertion

TWO TECHNICAL ISSUES MAY BE LISTED AS DISADVANTAGES:

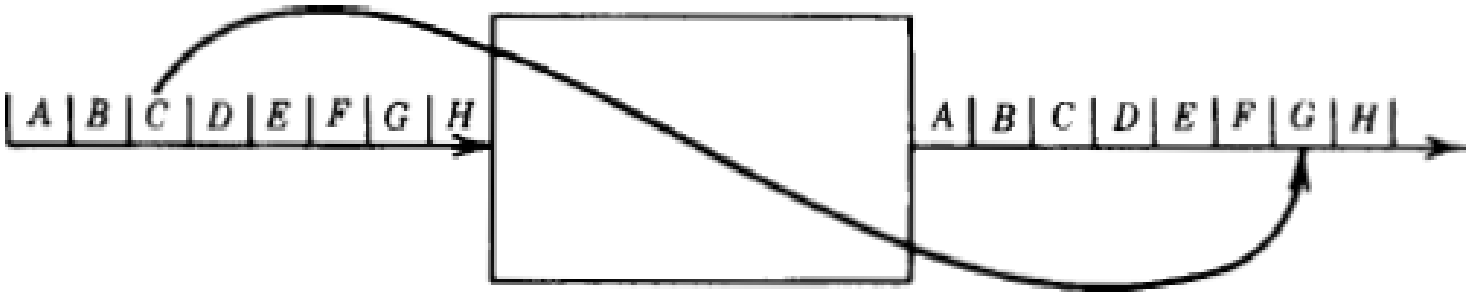
1. A digital switch deteriorates error performance of the system. A well-designed switch may only impact network error performance minimally, but it still does it.
2. Switch and network synchronization, and the reduction of wander and jitter, can be gating issues in system design.

Approaches to PCM Switching

- A digital switch's architecture is made up of two elements, called T and S, for time-division switching (T) and space-division switching (S), and can be made up of sequences of T and S.
- For example, the AT&T No. 4 ESS is a TSSSST switch; No. 3 EAX is an SSTSS; and the classic Northern Telecom DMS-100 is TSTS-folded. Many of these switches (e.g., DMS-100) are still available. One thing these switches have in common is that they had multiple space (S) stages. This has now changed. Many of the new switches, or enhanced versions of the switches have very large capacities (e.g., 100,000 lines) and are simply TST or STS switches.
- A simple time switch, a space switch, and methods of making up an architecture combining T and S stages are described ahead. Designing a switch with fairly high line and trunk capacity requires multiple stages.

TIME SWITCH

Time-slot interchanger (TSI): A time slot is the 8-bit PCM word. It expresses the voltage value of a sample taken at a certain moment in time. A time slot consists of 8 bits. A time-slot represents one voice channel, and the time slot is repeated 8000 times a second (with different binary values of course). DS1 has 24 time slots in a frame, one for each channel. E1 has 32 time slots.



A time-division switch, which we call a time-slot interchanger (TSI). Connectivity shown is from user C in the incoming slot C to user G in outgoing slot G.

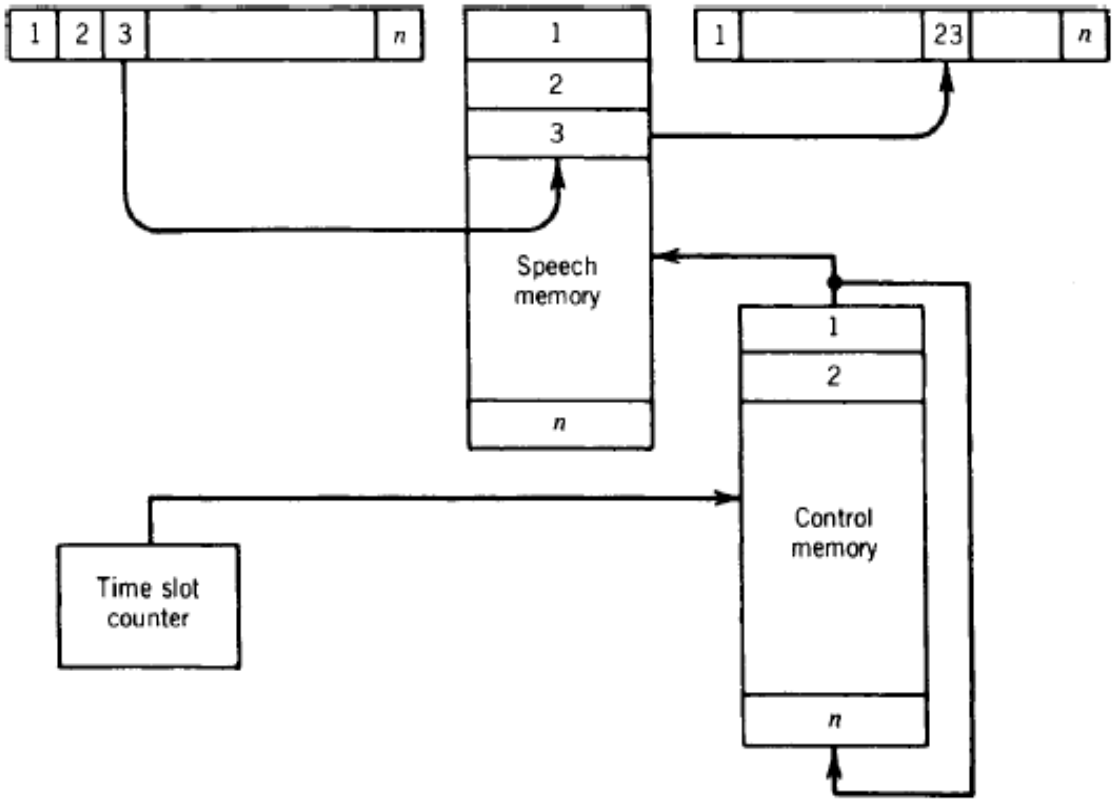
At least one time slot must be stored in memory (write) and then called out of memory in a changed position (read). The operations must be controlled in some manner, and some of these control actions must be kept in memory together with the software managing such actions. Typical control functions are timeslot “idle” or “busy.” Three of the basic functional blocks of a time switch:

1. Memory for speech
2. Memory for control

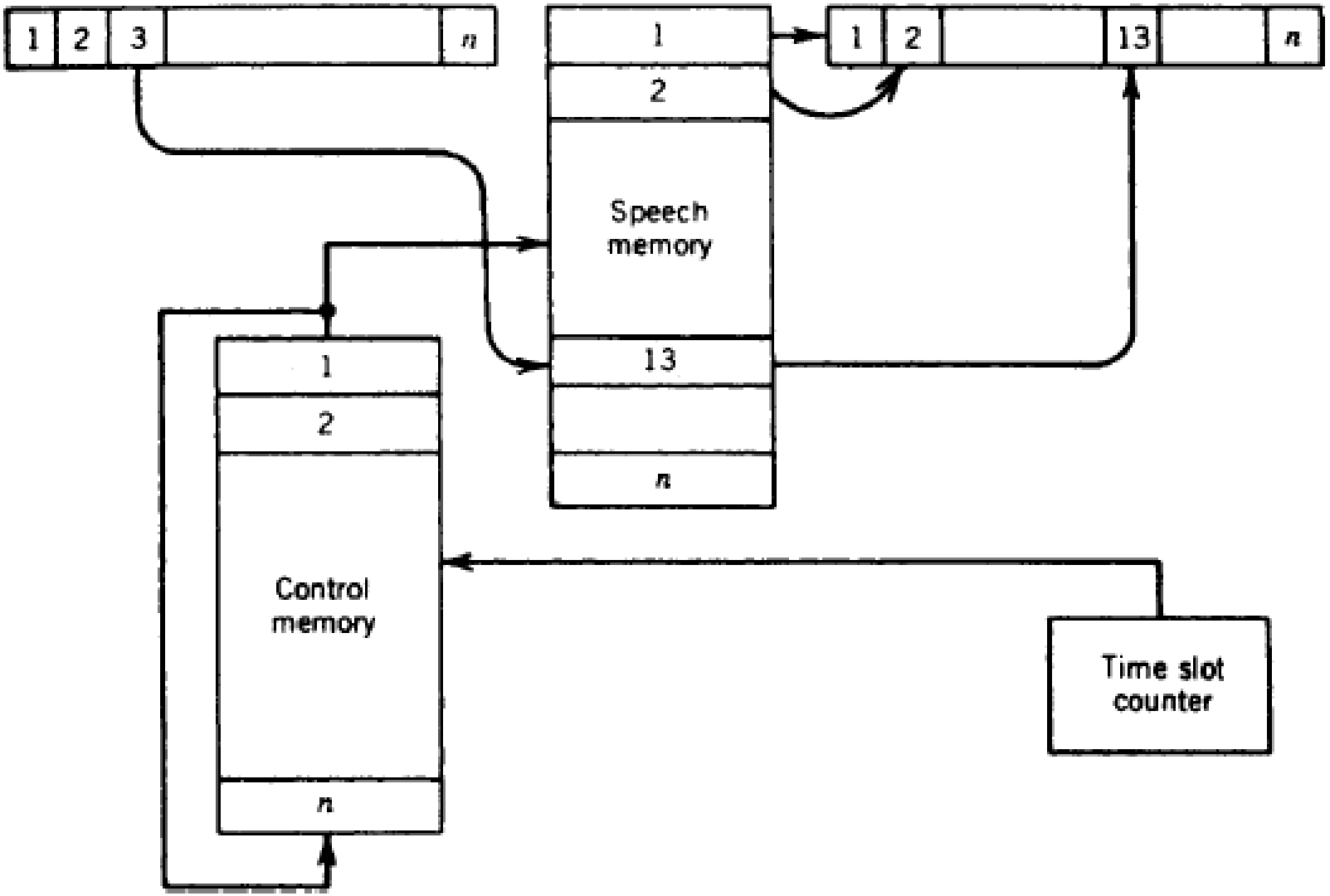
and

3. Time-slot counter or

processor



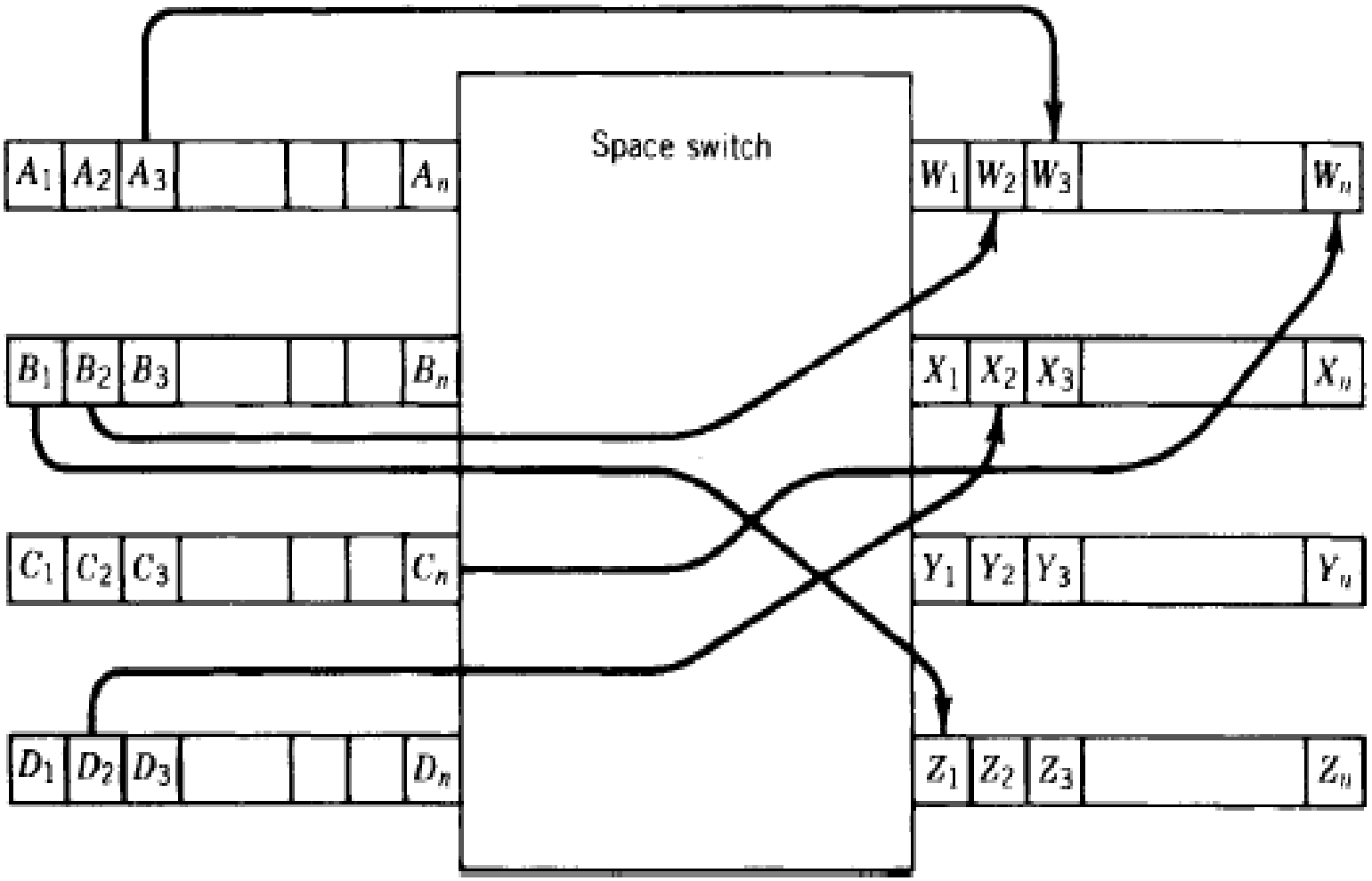
Time-slot interchange: time switch (T). Sequential write, random read.



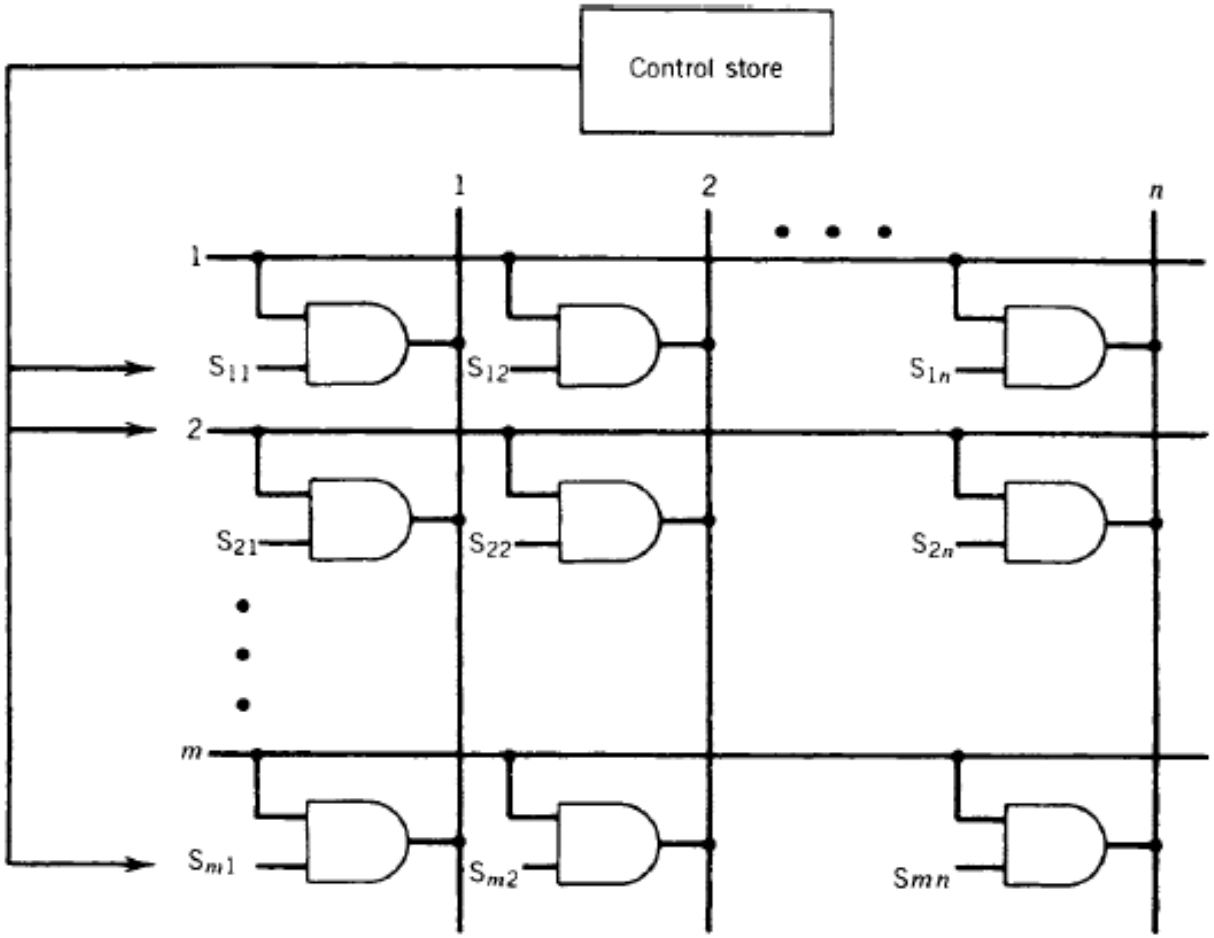
Time-switch, time-slot interchange (T). Random write, sequential read.

Space Switch

- It consists of a cross-point matrix made up of logic gates that allow the switching of time slots in a spatial domain. These PCM time slot bit streams are organized by the switch into a pattern determined by the required network connectivity.
- The matrix consists of a number of input horizontals and output verticals with a logic gate at each cross point. The array, as shown in the figure, has M horizontals and N verticals, and we call it an M× N array.
- If M = N, the switch is non blocking; If M > *N*, *the switch* concentrates, and if M < *N*, *the switch expands*.



Space switch connects time slots in a spatial configuration.



Time-division space switch cross-point array showing enabling gates.

The array consists of a number of (M) input horizontals and (N) output verticals. For a given time slot, the appropriate logic gate is enabled and the time slot passes from the input horizontal to the desired output vertical. The other horizontals, each serving a different serial stream of time slots, can have the same time slot (e.g., a time slot from time slots number 1–24, 1–30, or 1–n; e.g., time slot 7 on each stream) switched into other verticals enabling their gates.